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(54) **Failure tolerant memory device, in particular of the flash EEPROM type**

(57) Since fault phenomena such as lowering of the cell gain and cell emptying occur during normal operation the present invention proposes that in the memory device the row and/or column address decoding means (RDEC,CDEC) comprise at least one non-volatile memory (NVM) for address mapping and that the reading and writing control logic (CL) comprise means (TST) designed to identify cell faults in the rows and/or columns of the matrix (MAT) of the memory device and writing means (WM) designed to write on said non-volatile memory (NVM) during normal operation addresses corresponding to redundant rows and/or columns (RID) present in the matrix (MAT) to rectify said faults.

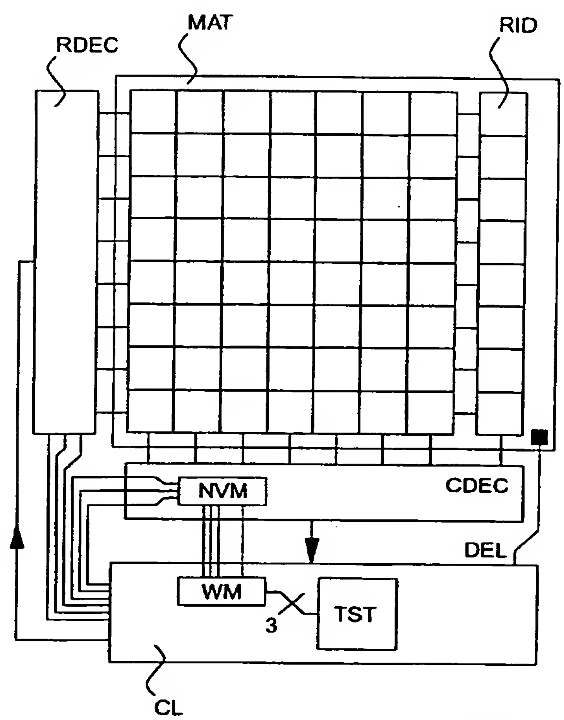

Fig.6

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The present invention relates to a memory device and in particular a flash EPROM in accordance with the preamble of claim 8 and a method for discriminating a gain-based insulated-gate single memorisation-transistor memory cell and to a method of deleting a memory cell of the same type. The memory device in accordance with the present invention can find advantageous application also in integrated circuits such as microprocessors and microcontrollers.

In the area of non-volatile semiconductor memories, presently comprising the UV_EPROM, E_EPROM and flash EPROM, the memory device consists of a matrix of equal cells which comprise for the memorisation of the data a single MOS transistor having at least one insulated gate. The value 0 or 1 of the data memorised depends on the amount of charges present on the insulated gate which in turn determines the threshold voltage of the MOS transistor.

As known, with the matrix must be connected row and/or column address decoding means and a control logic for reading, writing and deletion of the matrix cells.

There are often provided in the matrix one or more redundant rows and/or one or more redundant columns. These are used during manufacturing testing to obviate manufacturing defects by replacing the rows or columns containing faults with redundant rows or columns.

FIG. 1 shows a flash EPROM cell matrix with 2 rows and 3 columns.

Various well known mechanisms are used for the programming and deletion operation which can take place either globally, i.e. they affect the entire matrix, or selectively. The reading operation consists of applying to the selected cell a polarization voltage (for writing) and detecting the corresponding current (for writing) and in comparing it with appropriate reference currents.

In particular in flash EPROM memories, reading and programming are selective while deletion is done electrically and globally.

Almost always, the programming and deletion operations take place by means of a series of identical successive phases. For programming, injection of 'hot electrons' and, for deletion, extraction of charges by the Fowler-Nordheim effect. After each individual programming or deletion phase there is a phase of verification of the charge present on the insulated gate of each cell. In this manner the charge status and consequently the threshold voltage of the individual cells can be controlled with great precision.

FIG. 2 shows in a simplified manner the gate voltage versus channel current characteristics of cells having different charge status. In particular, A0 indicates the characteristic of a cell at instant t0 having a threshold voltage VT(t0) and gain G1 while A1 indicates the characteristic of the same cell at instant t1, following t0, after a deletion phase and thus having the same gain G1 but threshold voltage VT(t1) lower than VT(t0).

The verification phase consists of a particular reading operation performed with particular reference currents more restrictive than those used for the normal reading operation.

In flash EPROM devices it is extremely important that all the cells 'experience the same history', i.e. they must be programmed and deleted the same number of times. For this reason, before the actual deletion there is a programming operation of all the cells denominated 'preconditioning'.

After the 'preconditioning' operation, all the cells have a threshold voltage higher than a pre-set value VT0. The characteristic indicated by A2 in FIG. 2 having a reference gain G represents the limit of the programming condition while after the subsequent deletion operation all the cells have a threshold voltage lower than a pre-set value VT1. The characteristic indicated by A3 in FIG. 2 having the same reference gain G represents the limit of the deletion condition. The values Vt0 and VT1 depend on the manufacturing process and design choices. A possible choice could be 5V for VT0 and 2V for VT1 respectively.

Ideally all the memory cells are deleted with the same speed and hence, after the deletion operation the threshold voltage values of the various cells are found all in a small area slightly below the value VT1.

During laboratory experiments and manufacturing tests some phenomena were found which degrade the performance and life of flash EPROM devices.

There are cells which are deleted more rapidly than others. This phenomenon leads to the fact that when the deletion operation is completed their threshold voltage can be lowered much below VT1, as with the characteristic A5 and some times to a level, in general less than 0V as in the case of the characteristic A6, such as to become an irreversible lowering - 'emptied cell' or 'depleted bit'. This can generate errors during writing operations because said cells conduct current even when they are not selected.

There are cells which are deleted more slowly than others because their transconductance, and hence their gain and reading current, is lower than average. The characteristic indicated by A4 in FIG. 2 belongs to a cell of this type having gain G2. This phenomenon is found in manufacturing testing and during the life of the device and leads to the fact that when the deletion operation is terminated the cells having normal transconductance, i.e. nearly all, have reached extremely low threshold vol-

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tages often less than 0V. This leads to the shortcomings mentioned above and can also lead to degradation of a large part of the cell matrix. In addition it is also possible that the deletion operation will not end in the maximum time limits provided.

Heretofore it was sought to identify these situations and rectify them during manufacturing testing. The purpose of the present invention is to provide a method capable of identifying these situations during normal operation of the device and rectify them, in the light of the found and unexpected fact that they can arise even during the life of the device, and provide a memory device which would be tolerant of 'fault' situations like these and in particular gain lowering.

This purpose is achieved by a method for discrimination of a memory cell having the characteristics set forth in claim 1, by the method for deleting memory cells having the characteristics set forth in claim 3, and by a memory device having the characteristics set forth in claim 8. Additional advantageous aspects of the present invention are set forth in the dependent claims. In accordance with another aspect the present invention also concerns an integrated circuit having the characteristics set forth in claim 11.

Since fault phenomena such as those discussed occur during normal operation the present invention proposes that in the memory device the decoding means comprise at least one non-volatile memory for address mapping and that the control logic comprise means for identifying cell faults in the rows and/or columns of the matrix and writing means designed for writing on said non-volatile memory during normal operation addresses corresponding to the redundant rows and/or columns to rectify said faults.

In addition it is possible to not degrade the cell matrix even in the presence of lowered gain cells by foreseeing that these will be identified and that during the deletion operation the deletion status will occur only for the non-lowered gain cells.

The present invention is clarified by the following description together with the annexed drawings wherein:

FIG. 1 shows a memory cell matrix,

FIG. 2 shows in a simplified manner in a Cartesian voltage-current diagram the characteristics of some memory cells having different threshold voltages,

FIG. 3 shows in a simplified manner in a Cartesian voltage-current diagram the characteristics of some memory cells having different gains,

FIG. 4 shows a flow chart of a discrimination method in accordance with the present invention,

FIG. 5 shows a flow diagram of a deletion method in accordance with the present invention, and

FIG. 6 shows a block diagram of a memory device in accordance with the present invention.

FIG. 3 shows a series of characteristics of cells all having different gains and a common point P1 identified by the co-ordinates V1,I1, i.e. by applying the reading voltage V1 to all these cells there is obtained therefrom the same reading current I1 and the characteristics are indicated in decreasing order of gain and threshold voltage by B0 (with gain G0 and threshold voltage VT(B0)), B1 (with gain G1 and threshold voltage VT(B1)), B2 (with gain G2 and threshold voltage VT(B2)) respectively. The voltages Vt0 and VT1 keep the same meaning explained above.

The method in accordance with the present invention for discriminating on the basis of the gain a memory cell of the type with single insulated-gate memorisation transistor comprisEs the following phases:

a. carry the insulated gate of the cell in a charge state such that by applying a first reading voltage V1 to the cell by means of successive programming and/or deletion and verification phases there is detected a first reading current about equal to a first value I1 (as shown in FIG. 3),

b. apply a second reading voltage V2,

c. detect a second reading current I(B) opposite the second reading voltage V2,

d. compare the value of the second reading current I(B) with a second value I2 which together with the second reading voltage V2 identifies a point P2, and

e. associate the cell alternatively with a first or a second class of cells based on the outcome of said comparison.

Specifically for the purposes of the present invention it proved advantageous to have the second reading voltage V2, e.g. 6.25V, higher than the first reading voltage V1, e.g. 4.5V, the second value I2 higher than the first value I1, and the cell associated with a first class of high-gain cells if from said comparison it proved that said second reading current I(B) was higher than said second value I2 and otherwise with a second low-gain cell class.

The discrimination method can be rapidly understood by considering the description made together with the flow chart shown in FIG. 4, having the following block-actions correspondence:

100 method start
110 cell conditioning - phase a. of the method
101 apply V1
102 detect I(V1)
103 test on I(V1) in relation to I1
104 deletion phase
105 programming phase

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120 apply V2 - phase b. of the method
130 detect I(V2) - phase c. of the method
140 test on I(V2) in relation to I2 - phase d. of the method
150 high-gain association - end of method phase e.
160 low-gain association - end of method phase e.

The one shown in FIG. 3 could be the situation which appears in three cells of an EPROM flash memory device after phase a. of the method in accordance with the present invention. By applying to the three cells the second reading voltage V2 there will be detected the currents I(B0), I(B1), I(B2) respectively of which the first two are higher than the second value I2 while the last, i.e. I(B2), is not. For the purposes of the present method therefore the first three cells will be considered high-gain and the last low-gain. Graphically it can be seen that the characteristics slope reflects this situation.

It is specified lastly that the real form of the cell characteristics is not the rectilinear type but their qualitative behaviour, for the purposes of the graph and method, is the same.

It remains to be discussed how to perform practically in a physical memory device phase d. of the method, i.e. the current comparison. This can be done, e.g. by using a reference memory cell having the BRIF characteristic having a reference gain GRIF and brought to a threshold voltage VT-(BRIF) such that by applying thereto the second reading voltage V2 the reading current I2 is detected, and sending to a sense amplifier the currents of the reference cell and of the cell to be discriminated. Current comparisons by means of sense amplifiers and reference cells are used normally in reading operations and in programming and deletion verification phases using appropriate reference cells. Thus to discriminate the cells on the basis of gain basically no further circuitry in the memory device is necessary.

Since the low cell gain problem becomes, as explained above, particularly dangerous for the memory device when one prepares to delete it, the ideal moment for performance of a discrimination phase is concomitantly with the deletion operation.

As explained above, a conventional deletion operation of the cells of a memory device of the insulated-gate single-transistor memorisation type, in particular the EPROM flash type, consists of at least one series of successive individual deletion and verification phases of the cell deletion status.

The deletion method in accordance with the present invention comprises also at least one individual cell discrimination phase on the basis of the gain suitable for identifying the high-gain cells and provides that, after said discrimination phase, the individual verification phases affect only the high-gain cells.

In this manner it is avoided that many cells be 'depleted'.

The deletion method can be rapidly understood by considering the description given together with the flow chart shown in FIG. 5 and having the following block-actions correspondence and in which V3 and I3 indicate the voltage and current respectively on the basis of which the cell deletion condition is to be verified:

BlockAction
200 method start
210 gain test of cell G compared with Gmin
220 apply V3
230 detect I(V3)
240 test on I(V3) compared with I3
250 deletion phase
260 method end

In the example of FIG. 5 the discrimination phase - block 210 - precedes the actual cell deletion.

The discrimination phase can be provided by any method.

It is particularly advantageous to use the discrimination method in accordance with the present invention immediately after the 'preconditioning' and before the actual deletion because in this case, if a value of V1 lower than the value of VT0 is chosen, the discrimination phase already carries a partial but not dangerous deletion of the cells which thus shortens the actual deletion. As a whole then the deletion performed with the method of the present invention is not basically longer than that of the known art but considerably safer.

All these operations can affect the entire memory device or blocks thereof.

The cells which are not high-gain are considered faulty and possibly signalled as such to the user of the device. In a very simple case the user will avoid using them.

A more sophisticated version of the method provides that at least the faulty cells are replaced with redundant cells. More often it happens that the entire column or row to which they belong is replaced.

In this last case, for reasons of uniformity of use of all the cells of the matrix, it is well that all the redundant cells experience on average the same life as the non-redundant cells before their replacement. To achieve this it is necessary that the preconditioning and subsequent deletion affect always also the redundant cells.

It has been seen that various 'fault' phenomena affect the memory devices during their life and among these lowering of the cell gain.

There is not explained with the aid of FIG. 6 the memory device in accordance with the present invention which is fault tolerant. It comprises:

a.) matrix MAT of memory cells having a plurality of rows and columns of which at least one

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row and/or column RID is redundant,

b.) decoding means RDEC,CDEC for row and/or column addresses, and

c.) control logic CL for writing, reading and deletion of the cells and control of the device components.

The decoding means RDEC, CDEC comprise at least one non-volatile memory NVM for address mapping and the control logic CL comprises means TST designed to identify cell faults in the rows and/or columns and writing means WM designed to write on the non-volatile memory NVM, during normal operation of the device, addresses corresponding to said at least one redundant row and/or column RID to rectify said faults.

In the example of FIG. 6 there is a matrix MAT made up of 8 rows and 8 columns, only one redundant column RID, a 3-bit row decoder RDEC, a 3-bit column decoder CDEC, and a non-volatile memory NVM formed from 8 3-bit words, used only for mapping column addresses and included in the 3-bit column decoder CDEC.

From the control logic CL comes out the column address to be sent to the 3-bit column decoder CDEC, the row address to be sent to the 3-bit row decoder RDEC, and at least one signal DEL for the deletion to be sent to the matrix MAT. Furthermore it is connected to the input of the 3-bit row decoder RDEC and the input of the 3-bit column decoder CDEC. The means TST pilot the writing means WM which are connected in writing to the non-volatile memory NVM.

Initially the non-volatile memory NVM contains in order the following eight words: 000, 001, 010, 011, 100, 101, 110, 111.

When the means TST identify a 'fault' among those foreseen in a particular cell, they send to the writing means WM the column address corresponding to said faulty cell, e.g. 011. The writing means WM use this address to address the non-volatile memory NVM and use as writing data the column address corresponding to the redundancy column, in the example 111, and perform a writing operation on the non-volatile memory NVM.

At the end the non-volatile memory NVM contains in order the following eight words: 000, 001, 010, 111, 100, 101, 110, 111.

In the example there is no possibility of rectifying additional 'faults'.

The design and realization of such a control logic CL falls within the normal activities and abilities of those skilled in the art.

It is clear that control of the entire device is entrusted to the control logic CL which can be the wired or programmed type. For deletion, this can be pre-set to operate in accordance with the method of the present invention.

The means TST can be in particular individual discrimination means for the cells of the matrix MAT which can consist of logics of the wired or programmed type and operate, e.g. in accordance with the method of the present invention.

A fault tolerant memory device in accordance with the present invention can find an advantageous application in any integrated circuit where it is necessary to store data and/or programs.

Claims

1. Method of discriminating a memory cell of the single-transistor insulated gate memorization type and in particular of the EPROM type based on gain and comprising the following phases:

   a) carry the insulated gate of the cell in a charge state such that by applying a first reading voltage (V1) to the cell by means of successive programming and/or deletion and verification phases there is detected a first reading current about equal to a first value (I1),

   b) apply a second reading voltage (V2),

   c) detect a second current (I(B)) opposite the second reading voltage (V2),

   d) compare the value of the second reading current (I(B)) with a second value (I2), and

   e) associate the cell alternatively with a first or a second class of cells based on the outcome of said comparison.

2. Method in accordance with claim 1 in which said second reading voltage (V2) is higher than said first reading voltage (V1) and in which said second value (I2) is higher than said first value (I1) and in which said cell is associated with a first class of high-gain cells if from said comparison it proves that said second reading current (I(B)) is higher than said second value (I2) and otherwise is associated with a second class of low-gain cells.

3. Method of deleting cells of a memory device of the single-transistor insulated gate memorisation type and in particular the EP-ROM flash type by means of at least one series of successive deletion and individual verification phases of the cell deletion state and characterised in that it comprises at least one individual discrimination phase of said cells on the basis of the gain designed to identify the high-gain cells and in that, after said discrimination phase, said individual verification phases affect only the high-gain cells.

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4. Method in accordance with claim 3 in which said discrimination phase takes place in accordance with the method set forth in claims 1 or 2 before said series of successive deletion and verification phases.

5. Method in accordance with claim 3 or 4 in which the cells not high-gain are considered faulty.

6. Method in accordance with claim 5 in which at least said faulty cells are replaced by redundant cells.

7. Method in accordance with claim 6 in which said redundant cells experience on average the same life as the non-redundant cells before said replacement.

8. Memory device, in particular flash EPROM, of the type comprising:
   a.) matrix (MAT) of memory cells having a plurality of rows and columns of which at least one row and/or column (RID) is redundant,
   b) decoding means RDEC,CDEC for row and/or column addresses, and
   c.) control logic (CL) for writing, reading and deletion of the cells and control of the device components,

   characterized in that said decoding means (RDEC,CDEC) comprise at least one non-volatile memory (NVM) for mapping said addresses and that said control logic (CL) comprises means (TST) designed to identify cell faults in said rows and/or columns and writing means (WM) designed to write on said non-volatile memory (NVM) during normal operation of said device addresses corresponding to said at least one redundant row and/or column (RID) to rectify said faults.

9. Device in accordance with claim 8 in which said control logic (CL) comprises additionally discrimination means (TST) for said cells on the basis of gain and designed to pilot said writing means (WM),

10. Device in accordance with claim 9 in which said control logic (CL) operates for deletion in accordance with the method set forth in one of the claims from 3 to 7.

11. Integrated circuit comprising a memory device for storing data and/or programs characterised in that said memory device is the type set forth in claims 8 to 10.

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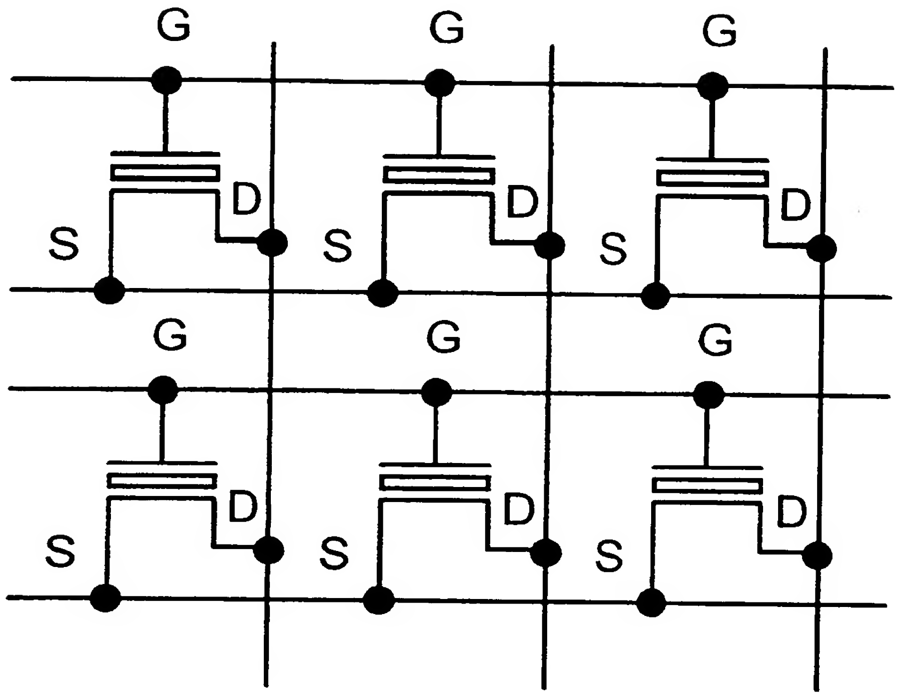

Fig.1

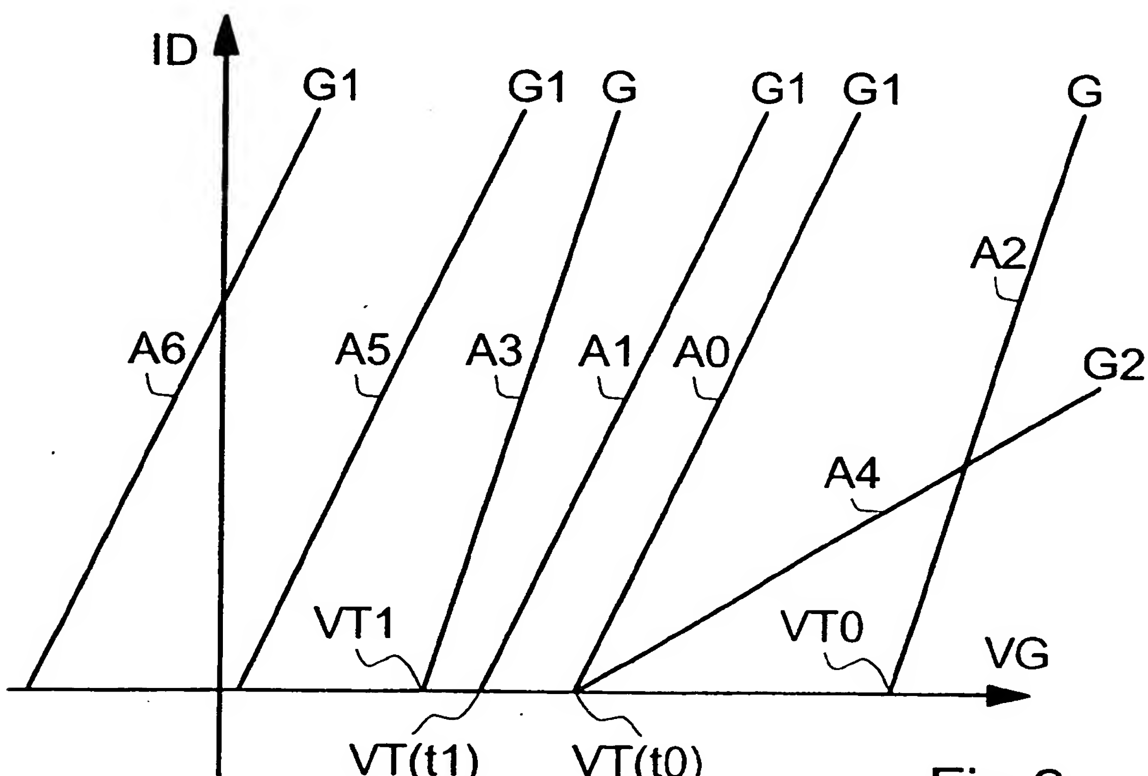

Fig.2

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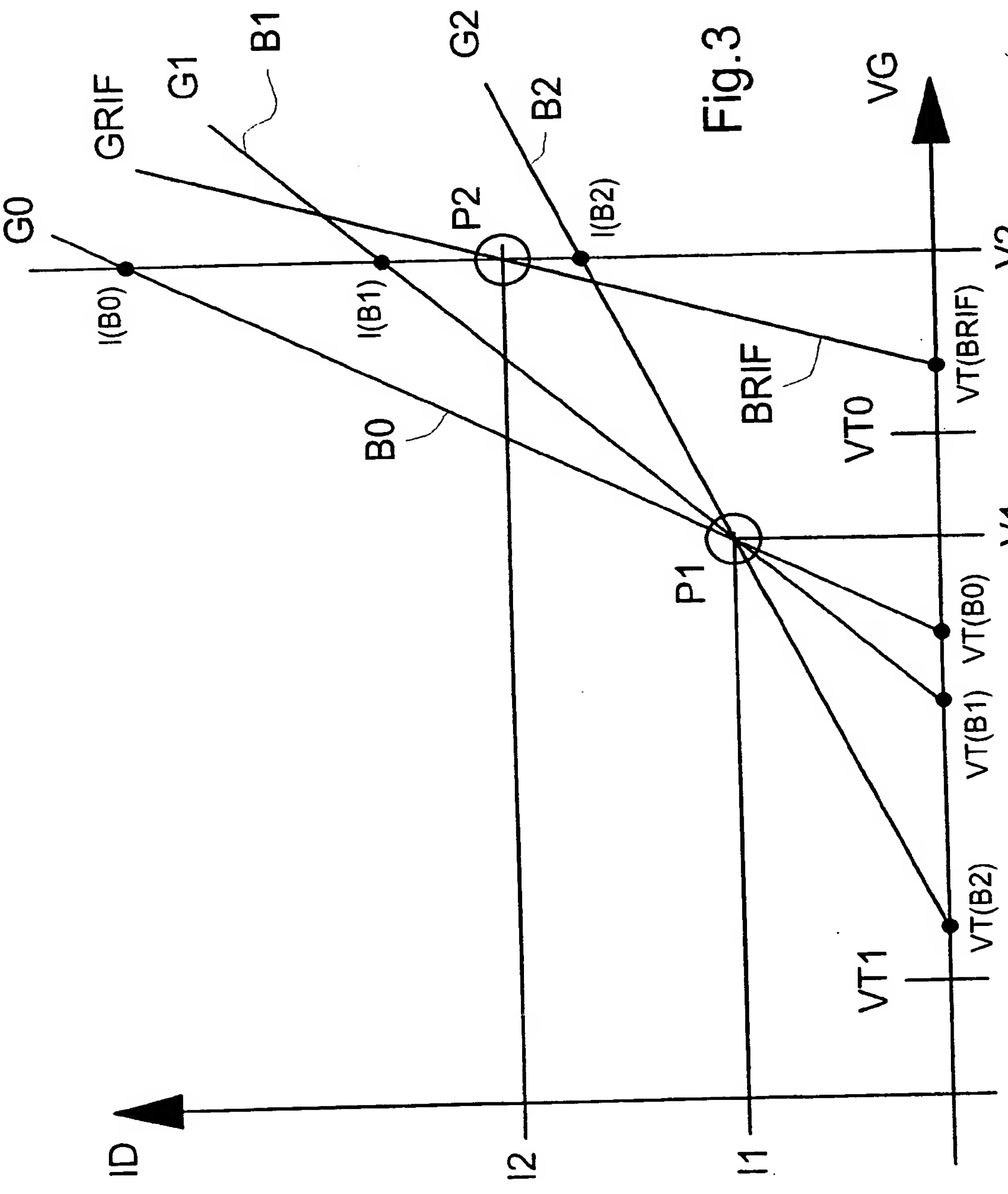

Fig.3

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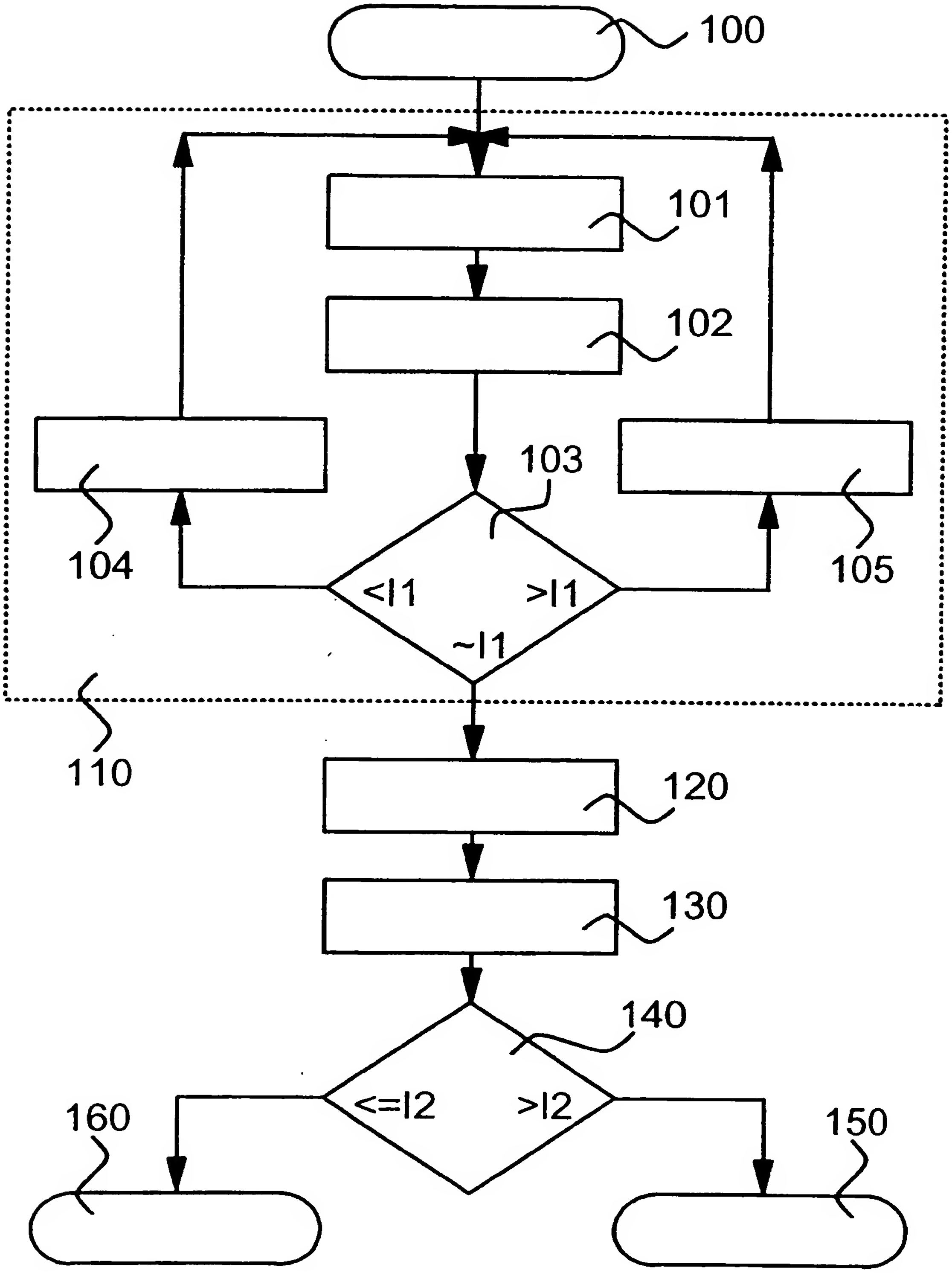

Fig.4

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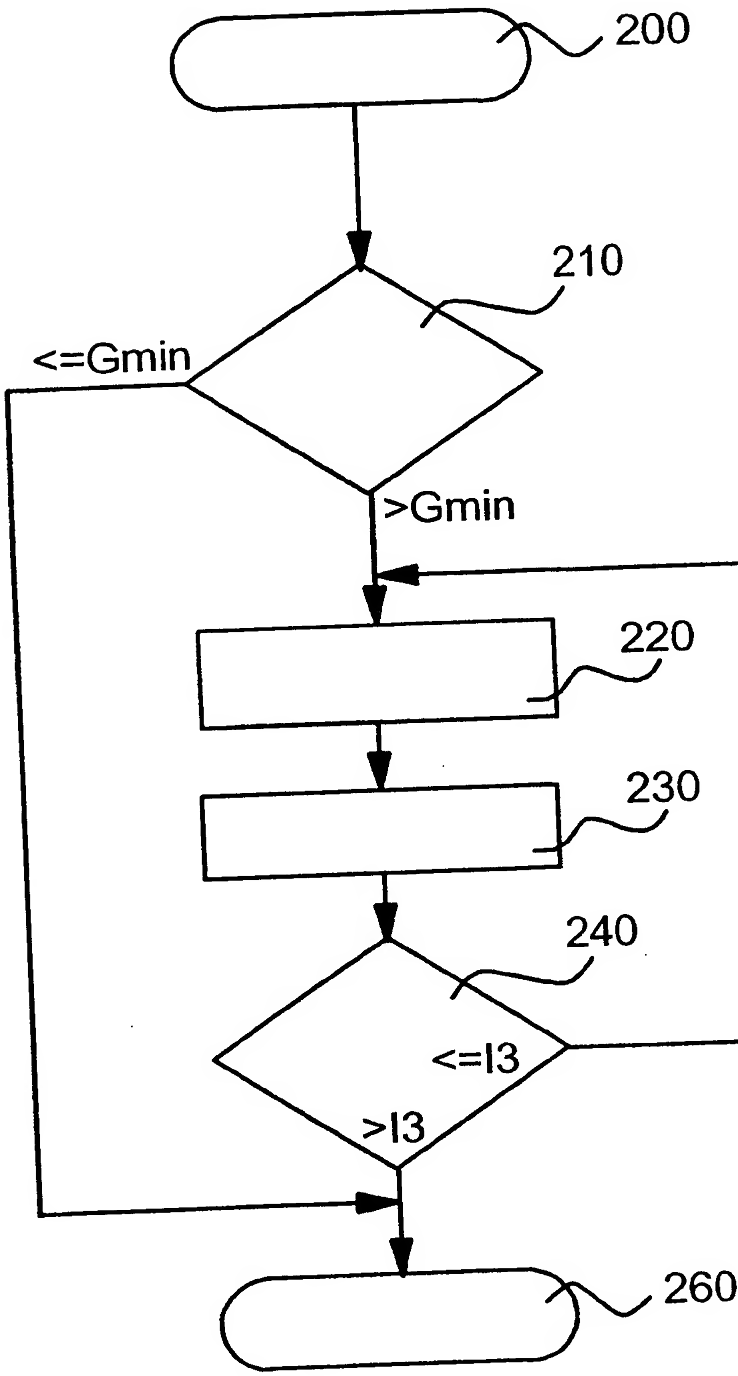

Fig.5

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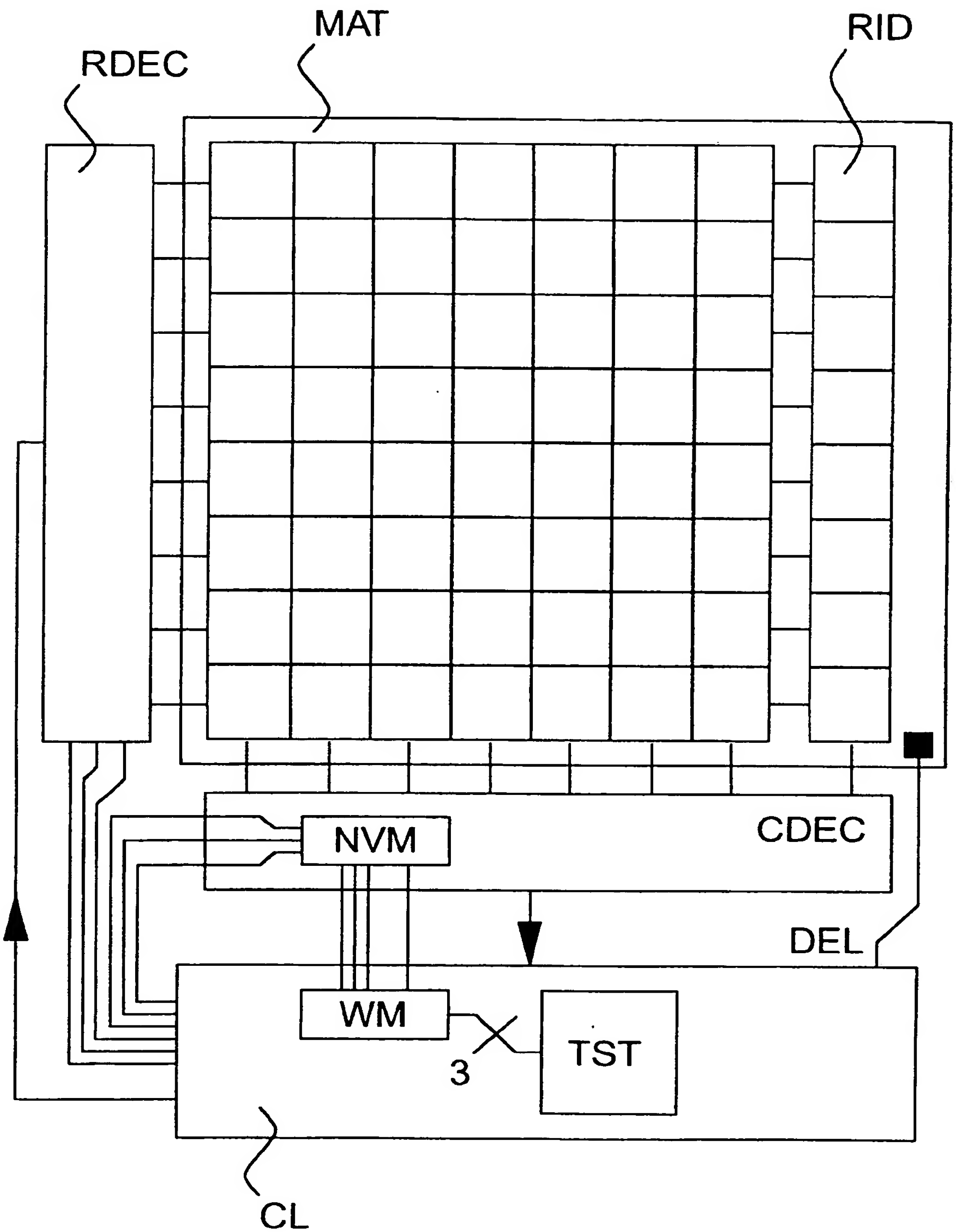

Fig.6

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EUROPEAN SEARCH REPORT

Application Number
EP 94 83 0283

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	FR-A-2 694 404 (SGS THOMSON MICROELECTRONICS-FR) * the whole document * ---	1	G11C29/00 G11C16/06 G06F11/20
A	DE-A-42 07 934 (KABUSHIKI KAISHA TOSHIBA) * the whole document * ---	1	
A	US-A-4 779 272 (KOHDA ET AL.) * claims 1,5 * ---	1	
A	EP-A-0 403 822 (TEXAS INSTRUMENTS INCORPORATED) * abstract * ---	1	
X	WO-A-94 07211 (SUNDISK CORPORATION) * the whole document * ---	8	
A	GB-A-2 254 173 (INTEL CORPORATION) * abstract * ---	8	TECHNICAL FIELDS SEARCHED (Int.Cl.6)
A	US-A-4 733 394 (GIEBEL) * the whole document * ---	8	G11C G06F
A	EP-A-0 548 866 (NEC CORPORATION) ---		
A	EP-A-0 600 151 (FUJITSU LIMITED) -----		

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	16 December 1994	Absalom, R

CATEGORY OF CITED DOCUMENTS

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